REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application and indicating that claims 1-14, 19, and 20 are allowable.

I. Disposition of Claims

Claims 1-20 are currently pending in the present application. By way of this reply, claim 15 has been amended.

II. Claim Amendments

Claim 15 has been amended to recite that the creating of the wire load model comprises selecting an error bound for a curve-fitting process. No new matter has been added by way of this amendment as support for this amendment may be found, for example, in paragraph [0025] of the Specification.

III. Allowed Claims

Claims 1-14, 19, and 20 have been allowed. Applicant thanks the Examiner for carefully considering and allowing these claims.

IV. Rejection(s) Under 35 U.S.C § 112

Claims 15-18 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Application regards as the invention. Specifically, the Examiner indicated that

claim 15 failed to provide sufficient antecedent basis for the phrase "the creating" appearing at the end of claim 15. By way of this reply, the instance of "the creating" referred to by the Examiner has been removed from claim 15, and thus, the § 112, second paragraph rejection is now moot.

V. Rejection(s) Under 35 U.S.C § 102

U.S. Patent No. 5,629,860

Claims 15-18 of the present application were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,629,860 issued to Jones et al. (hereinafter "Jones"). For the reasons set forth below, this rejection is respectfully traversed.

The present invention is directed to a technique for generating a wire load model that is useful for timing and noise analyses in an early integrated circuit design stage. The wire load model is derived by the simulation of wires in different layers to obtain parasitic information, which is then curve-fitted to produce the wire load model. As required by amended independent claim 15 of the present application, the creation of the wire load model comprises selecting an error bound for a curve-fitting process. Thus, such a curve-fitting process has an error control mechanism by which an error bound may be specified for a particular curve-fitting. *See* Specification, paragraph [0025]. In one exemplary embodiment of the present invention, via Equations (1)-(4) presented in paragraph [0024] of the Specification, the curve-fitting process allows one to control error by specifying the amount of error that can be tolerated.

Jones, in contrast to the present invention, fails to disclose, or otherwise teach, the present invention as recited in amended independent claim 15 of the present application.

Jones, which is directed to a method for determining timing delays of an integrated circuit layout, discloses that average wire length and average wire length variability data as a function of area information is curve fit to an empirically derived formula known as Rent's rule. *See* Jones, column 5, lines 49 – 53. However, Jones fails to show how one or ordinary skill in the art could adjust or control the curve fitting to account for error tolerance as this would be an important feature for newer technologies. In other words, Jones is completely silent as to how to provide an error tolerance for the curve fitting. Instead, Jones describes how to create a netlist for timing analysis purposes with the only constraints disclosed being design constraints (*see* Jones, column 6, lines 17 – 27), which are entirely distinct from an error bound for a curve-fitting process as required by amended independent claim 15.

In view of the above, Jones fails to show or suggest the present invention as recited in amended independent claim 15 of the present application. Thus, amended independent claim 15 of the present application is patentable over Jones. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

U.S. Patent No. 5,694,344

Claims 15, 16, and 18 of the present application were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,694,344 issued to Yip et al. (hereinafter "Yip"). For the reasons set forth below, this rejection is respectfully traversed.

Yip, like Jones, fails to disclose the present invention as recited in amended independent claim 15 of the present application. Yip, which is directed to modeling a

semiconductor package, discloses a semiconductor package modeling program that inputs a physical description of a semiconductor package and calculates a model comprising a resistor, inductor, and capacitor dependent on the description of the semiconductor package. *See* Yip, column 3, lines 58 – 67. However, Yip is completely silent as to selecting an error bound for a curve-fitting process as part of creating the wire load model as required by amended independent claim 15 of the present application.

In view of the above, Yip fails to show or suggest the present invention as recited in amended independent claim 15 of the present application. Thus, amended independent claim 15 of the present application is patentable over Yip. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

U.S. Patent No. 6,175,947

Claims 15-18 of the present application were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,175,947 issued to Ponnapalli et al. (hereinafter "Ponnapalli"). For the reasons set forth below, this rejection is respectfully traversed.

Ponnapalli, like Jones and Yip, fails to disclose the curve-fitting "error bound" limitation of amended independent claim 15 of the present application. Ponnapalli, which is directed to a method for extracting 3-D capacitance and inductance parasitics, discloses a purported curve-fitting process that approximates models with low-order polynomials. *See* Ponnapalli, column 8, lines 26 – 28. However, Ponnapalli is completely silent as to how to select an error bound for this modeling. With respect to the portions of Ponnapalli relied on in the Office Action dated October 21, 2003 as

disclosing selecting an error bound (namely, column 12, lines 4 - 6 of Ponnapalli), Ponnapalli describes a correction term that is simply added to a determined capacitance value in the case of deviant capacitance values. This is entirely distinct from controlling an error bound of a curve-fitting process used to generate a wire load model as required by amended independent claim 15 of the present application.

In view of the above, Ponnapalli fails to show or suggest the present invention as recited in amended independent claim 15 of the present application. Thus, amended independent claim 15 of the present application is patentable over Ponnapalli. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

U.S. Patent No. 6,291,254

Claims 15-18 of the present application were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,291,254 issued to Chou et al. (hereinafter "Chou"). For the reasons set forth below, this rejection is respectfully traversed.

Chou, like Jones, Yip, and Ponnapalli, fails to disclose the present invention as recited amended independent claim 15 of the present application. Chou, which is directed to techniques for determining integrated circuit process parameters, is altogether not directed to creating a wire load model, and therefore, cannot disclose a curve-fitting process to create a wire load model or selecting an error-bound for such a curve-fitting process. With respect to the portions of Chou relied on in the Office Action of October 21, 2003 (namely, column 9, lines 2 - 3 of Chou), Chou is clearly referring to field solvers, not curve-fitting processes. As is apparent from the claims of the present

invention, field solvers are distinct from curve-fitting processes. Moreover, as described in Chou, the field solver reiterates until a converged value of an interconnect process parameter is obtained. This is distinct from the selecting of an error bound for a curve-fitting process as required by amended independent claim 15 of the present application.

In view of the above, Chou fails to show or suggest the present invention as recited in amended independent claim 15 of the present application. Thus, amended independent claim 15 of the present application is patentable over Chou. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

VI. Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.102001; P5991).

Respectfully submitted,

Date: 12/10/03

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